UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/799,574	03/12/2004	Edmund Coersmeier	60282.00173	6496

32294 7590 04/18/2007
SQUIRE, SANDERS & DEMPSEY L.L.P.
14TH FLOOR
8000 TOWERS CRESCENT
TYSONS CORNER, VA 22182

EXAMINER	
FOTAKIS, ARISTOCRATIS	

ART UNIT	PAPER NUMBER
2611	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/18/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

PTOL-90A (Rev. 10/06)

Office Action Summary	Application No.	Applicant(s)	
	10/799,574	COERSMEIER, EDMUND	
	Examiner	Art Unit	
	Aristocratis Fotakis	2611	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *03/12/2004, 01/23/2006*.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 15 – 17 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The claimed invention does not fall within at least one of the four categories of patent eligible subject matter recited in 35 U.S.C. 101 (process, machine, manufacture, or composition of matter) and is directed to a computer program.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1 – 2, 5 – 10, 13 – 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coersmeier et al ("*Frequency selective IQ Phase and Amplitude Imbalance Adjustments for OFDM Direct Conversion Transmitters*" Proceedings of the International Symposium on Advanced Radio Technologies, March 4 – 7, 2003, Nokia, Bochum, Germany) in view of Yuda et al (US 2005/0018597)

Re claims 1, 6, 9, 14 and 15, Coersmeier teaches of an error adjustment system and method for equalizing transmission characteristics of a signal processing circuitry (Fig.1 and 4), the system comprising: generating means for generating an original complex IQ signal (Page 33, Col 2, Paragraph 3, Lines 1 – 6, Fig.1); error correction means for performing error correction on the original complex IQ signal of a respective signal branch by means of a correction function (Page 33, Col 2, Paragraph 3, Lines 6 – 11, Fig.1); signal processing circuitry for processing the corrected complex IQ signal of the respective signal branch, thereby obtaining a processed real signal of the respective signal branch (Page 34, Col 1, Paragraph 1, Fig.1); and a processing device comprising: receiving means for receiving an original complex IQ signal by the

generating means (Page 34, Col 1 - 2, Paragraph 3, Lines 6 – 8, Fig.1) and a processed real signal (Page 34, Col 1, Paragraph 2, Lines 7 – 12, Fig.1) of the signal branch; first calculating means for (*IQ estimation block*, Fig.1) calculating a processed complex IQ signal of the signal branch (output from the block, Fig.1) from the processed real signal (output from analog measurement block, Fig.1, Fig.4, Page 34, Col 1, Paragraph 2, Lines 7 – 12) and the original complex IQ signal of the signal branch (Fig.4, DSP, Page 36, Col 2, Paragraph 2 - 3); second calculating means (IQ Amplitude Error Detection block, Fig.1) for calculating a difference between the processed complex IQ signal and the original complex IQ signal (Page 36, Col 1, Paragraphs 1 and 2, equations (6)); third calculating means for calculating control values of a correction function (*correction coefficients*) of the signal branch on the basis of the difference (*errors*) calculated by the second calculating means (Page 34, Col 2, Paragraphs 1); and supplying means for supplying the control values calculated by the third calculating means to the correction function of the signal branch (to the adaptive IQ Amplifier Pre-Equalizer, Fig.1, Fig.4), wherein the receiving means, the first to third calculating means and the supplying means are configured to repeat their operations (feedback loop, Fig.1, Fig.4 and equation (7)). However, Coersmeier only teaches of one branch.

Yuda teaches of a transmission weight computing section that computes a transmission weight for directional transmission using an OFDM signal. A transmission correcting value memory section stores one correcting value for correcting the transmission weight for each sub-carrier of an OFDM signal or each band gathering a plurality of sub-carriers. A transmission weight correcting section corrects the

transmission weight by the correcting value. A transmitting branch weights transmission data by a transmission weight outputted from the transmission weight correcting section on a sub-carrier-by-sub-carrier basis and delivers it to an antenna (Abstract, Fig.5).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have used the branch configuration described by Coersmeier in a transmitter with a plurality of branches for increasing the traffic capacity, broadening the communication area, suppressing the interference (Col 1, Paragraph [0002], Lines 4 – 6).

Re claims 2 and 10, Coersmeier teaches of detecting means according to the signal branch, for detecting an envelope of the processed real signal (Figs.1 and 4, Analog Signal Measurement, Page 34, Col 1, Paragraph 2, Lines 1 - 7), wherein the receiving means of the processing device are configured to receive the original complex IQ signal of the signal branch generated by the generating means and the envelope of the processed real signal of the signal branch (Fig.4, DSP, Page 36, Col 2, Paragraph 2 - 3), and wherein the first calculating means are configured to calculate a processed complex IQ signal of the signal branch from the envelope of the processed real signal and the original complex IQ signal of the signal branch (see claim 1).

Re claims 5 and 13, Coersmeier teaches of the third calculating means configured to approximate a gradient of the difference calculated by the second

calculating (equations (6)) means on the basis of the difference and an approximation of a transmission characteristic of the signal processing circuitry of the signal branch (Page 36, Col 1, Lines 1 – 5), and to update control values of the correction function based on the approximated gradient, and wherein the supplying means are configured to supply the updated control values to the correction function of the signal branch (equation (7), Page 36, Col 1, Lines 5 – 7).

Re claims 7 and 8, Coersmeier teaches of the receiving means and the supplying means formed by a data bus (Data Bus, Fig.4), and wherein the first to third calculating means formed by a digital signal processor (DSP, Fig.4) and further comprising storage (Data & Information Memory block, Fig.4) means for storing algorithms to be carried out by the digital signal processor. (Page 36, Col 1, Paragraph 5, Col 2, Paragraph 2).

Re claims 16 and 17, Coersmeier teaches of the computer program product (Page 36, Col 1, Paragraph 4) wherein the computer program product comprises a computer-readable medium on which the software code portions are stored directly loadable into an internal memory of the computer (Data & Information Memory block, Fig.4) (Page 36, Chapter VII).

Claims 3 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coersmeier and Yuda as applied to claims 2 and 10 above, and further in view of Heiskala et al.(US 6,700,453).

Coersmeier and Yuda teach of all the limitations of claims 2 and 10. Coersmeier also teaches of calculating the new coefficients at time $n+1$ from the current coefficients at the time n (equation (7)). However, Coersmeier and Yuda do not specifically teach of comparing the envelope of the processed real signal with the envelope of the original IQ signal at the two consecutive time instances (n, n+1), to obtain the processed complex IQ signal.

Heiskala teaches of a method and an arrangement for compensating for amplitude imbalance of a quadrature modulator including: determining a first correlation (comparison, 51A, Fig.4) on the basis of a first modulation signal (ideal I signal, S_I, Fig.4) and an output signal of the quadrature modulator (processed real signal, P_{RF}, Fig.4); determining a second correlation (comparison, 51B, Fig.4) on the basis of a second modulation signal (ideal Q signal, S_Q, Fig.4) and the output signal of the quadrature modulator (processed real signal, P_{RF}, Fig.4); producing a compensation signal proportional to the amplitude imbalance on the basis of a ratio of the determined correlations and the first and second modulation signals; and processing at least one of the modulation signals of the quadrature modulator with the compensation signal;

wherein determining the correlations uses unprocessed modulation signals of the quadrature modulator for determining the correlations (Abstract, Fig.4).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have used the two correlators to remove the effect phase imbalance and the transmitter gain from the estimated error.

Claims 4 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coersmeier, Yuda and Heiskala as applied to claims 3 and 11 above, and further in view of Shirali (US 7,085,330).

Coersmeier, Yuda and Heiskala teach of all the limitations of claims 3 and 11 except for synchronization.

Shirali teaches of a signal processing method and apparatus capable of correcting signal distortion introduced by an RF power amplifier (#120, Fig.1), which includes the use of a buffer (#170, Fig.1) to store a plurality of samples representing at least a portion of an input signal intended for amplification by the RF power amplifier, the use of a self-receiver (#132, Fig.1) to receive an output signal generated by the RF power amplifier, the use of a synchronization unit (#165, Fig.1) to determine, as a matching input sample, which of the stored plurality of samples corresponds most closely to the output signal, and the use of a predistortion unit (#105, Fig.1) to selectively apply a distortion correction function to the input signal prior to amplification

by the RF power amplifier in which the distortion correction function being derived from a relationship between the matching input sample and the output signal (Abstract, Lines 1 – 15). The realized sample of the self-received signal are synchronized through correlating this realized sample against the contents of the buffer (#170). The synchronization unit (#165) is provided that, during its active phase it will take the I and Q components of this stored transmit signals (ideal IQ signal, Z_k . . . Z_{k-N}, Fig.1) derive the magnitude for each of the stored transmit signals and correlate the generated magnitudes against the magnitude of the realized sample of self-received signal (processed real signal, $|Z_{ADC}|$).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have used the synchronization unit to permit more precise and updateable determination of the delays involved in the RF modulation and amplification stages of the amplifier and the self-receiver, thus allowing for more precise and aggressive adaptive predistortion to be used (Abstract, Lines 15 – 20).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aristocratis Fotakis whose telephone number is (571) 270-1206. The examiner can normally be reached on Monday - Thursday 7 - 5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AF

CHIEH M. FAN
SUPERVISORY PATENT EXAMINER